

WHAT IS CLAIMED IS:

1 1. A trenched DMOS device having a termination structure, the trenched
2 DMOS device comprising:

3 a silicon substrate of a first conductive type, having a first epitaxial layer of
4 the first conductive type and a second epitaxial layer of a second conductive type formed
5 thereon;

6 a DMOS trench, formed in the first epitaxial layer and the second epitaxial
7 layer;

8 a first trench, formed in the first epitaxial layer and the second epitaxial layer
9 disposed close to an edge of the second epitaxial layer, the first trench to be utilized as a main
10 portion of the termination structure having a bottom disposed in the first epitaxial layer;

11 a second trench disposed between the DMOS trench and the first trench, the
12 second trench having another bottom disposed in the second epitaxial layer adjacent to a
13 region of the second conductive type;

14 a gate oxide layer on the DMOS trench and the first trench, the gate oxide
15 layer having extended portions covering an upper surface of the second epitaxial layer
16 adjacent the DMOS trench and of the second epitaxial layer adjacent the first trench;

17 a first polysilicon layer, formed in the DMOS trench;

18 a second polysilicon layer, formed over the gate oxide layer in the first trench,
19 having another extended portion covering the upper surface of the second epitaxial layer
20 adjacent the first trench, the second polysilicon layer having an opening to expose the gate
21 oxide layer disposed at the bottom of the first trench to split the second polysilicon layer into
22 two discrete parts;

23 an isolation layer, formed on the first polysilicon layer in the DMOS trench
24 and extended portions of the gate oxide layer adjacent the DMOS trench, on the second
25 polysilicon layer, and on the gate oxide layer over the second epitaxial layer at the bottom of
26 the first trench, the isolation layer having a first contact window to expose the second
27 polysilicon layer over the second epitaxial layer and a second contact window to expose the
28 second trench; and

29 a source metal contact layer, formed over the isolation layer and filling both
30 the first contact window and the second contact window, having a connection with a source
31 of the DMOS device and further having an edge beside the first contact window.

1 2. The trenched DMOS device of claim 1, wherein the isolation layer
2 includes a plurality of body contact windows extending into the second epitaxial layer, and
3 wherein the source metal contact layer is formed over the body contact windows.

1 3. The trenched DMOS device of claim 1, further comprising a drain
2 metal contact layer formed on a backside surface of the silicon substrate.

1 4. The trenched DMOS device of claim 1, wherein the isolation layer
2 comprises doped silicate glass.

1 5. The trenched DMOS device of claim 1, wherein the source metal
2 contact layer comprises a stack of Ti, TiN, and AlSiCu alloy.

1 6. The trenched DMOS device of claim 1, wherein the first conductive
2 type is an N type and the second conductive type is a P type.

1 7. The trenched DMOS device of claim 1, wherein the first conductive
2 type is a P type and the second conductive type is an N type.

1 8. A trenched DMOS device having a termination structure, the trenched
2 DMOS device comprising:

3 a silicon substrate of a first conductive type, having a first epitaxial layer of
4 the first conductive type and a second epitaxial layer of a second conductive type formed
5 thereon;

6 a pair of DMOS gates, formed in the first epitaxial layer and the second
7 epitaxial layer and being spaced by a body contact window;

8 a first trench, formed in the first epitaxial layer and the second epitaxial layer
9 disposed close to an edge of the second epitaxial layer, the first trench to be utilized as a main
10 portion of the termination structure having a bottom disposed in the first epitaxial layer;

11 a second trench disposed between the DMOS gates and the first trench, the
12 second trench having a bottom disposed in the second epitaxial layer adjacent to a region of
13 the second conductive type;

14 a gate oxide layer on the first trench, the gate oxide layer having extended
15 portions covering an upper surface of the second epitaxial layer adjacent the first trench;

16 a second polysilicon layer, formed over the gate oxide layer in the first trench,
17 having another extended portion covering the upper surface of the second epitaxial layer
18 adjacent the first trench, the second polysilicon layer having an opening to expose the gate
19 oxide layer disposed at the bottom of the first trench to split the second polysilicon layer into
20 two discrete parts;

21 an isolation layer, formed on the DMOS gate, on the second polysilicon layer,
22 and on the gate oxide layer over the second epitaxial layer at the bottom of the first trench,
23 the isolation layer having a first contact window to expose the second polysilicon layer over
24 the second epitaxial layer and a second contact window to expose the second trench; and

25 a source metal contact layer, formed over the isolation layer and filling both
26 the first contact window and the second contact window, having a connection with a source
27 of the DMOS device and further having an edge beside the first contact window.

1 9. The trenched DMOS of claim 8 wherein the pair of gates are spaced by
2 a bipolar transistor structure.

1 10. The trenched DMOS of claim 8 wherein the source metal contact layer
2 is formed over the body contact windows.

1 11. A fabrication method of forming a DMOS device and a termination
2 thereof comprising:

3 forming a first epitaxial layer of a first conductive type over a silicon substrate
4 of the first conductive type;

5 forming a second epitaxial layer of a second conductive type over the first
6 epitaxial layer;

7 patterning and etching the first and second epitaxial layers to form a plurality
8 of DMOS trenches and a first trench, the DMOS trenches and the first trench having bottoms
9 disposed in the first epitaxial layer;

10 forming a gate oxide layer over the exposed surface by thermal oxidation;
11 forming a polysilicon layer over all the exposed surfaces to fill the DMOS
12 trenches;

13 patterning and etching the polysilicon layer to form a plurality of gate
14 electrodes and a termination polysilicon layer, and the termination polysilicon layer having
15 an opening to expose a bottom surface of the first trench and an extended portion covering
16 the second epitaxial layer adjacent to the first trench;

17 forming a photoresist pattern to define source regions and forming the source
18 regions of the first conductivity type;
19 forming an isolation layer over the exposed surfaces;
20 patterning and etching the isolation layer to form a plurality of body contact
21 windows over the source regions, a second contact window over the second epitaxial layer
22 between the first trench and the DMOS trench, and a first contact window over the extended
23 portion of the termination polysilicon layer;
24 implanting dopants of a second conductive type through the body contact
25 windows and the second contact window;
26 forming a source metal contact layer over the exposed surface to fill the body
27 contact windows, first contact window, and the second contact window; and
28 patterning and etching to remove the source metal contact layer over the
29 termination structure.

1 12. The method of claim 11, further comprising providing on a backside
2 surface of the silicon substrate a drain metal contact layer.

1 13. The method of claim 11, wherein the DMOS trench has a width of
2 about 0.15~1.5 micron.

1 14. The method of claim 11, , wherein the first trench has a width of about
2 5~50 micron.

1 15. The method of claim 11, wherein the gate oxide layer has a thickness
2 of about 15~100 nm.

1 16. The method of claim 11, wherein patterning and etching the isolation
2 layer to form the body contact windows, the second contact window, and the first contact
3 window comprises:

4 etching the isolation layer and the gate oxide layer to expose the source
5 regions for the body contact windows and to expose the second epitaxial layer for the second
6 contact window, and etching the isolation layer to expose the extended portion of the
7 termination polysilicon layer to form the first contact window; and

8 etching the exposed source regions to form the body contact windows, and the
9 exposed second epitaxial layer to form the second contact window.

1 17. The method of claim 16, wherein etching the isolation layer and the
2 gate oxide layer comprises using the source regions, the second epitaxial layer, and the
3 termination polysilicon layer as etch stop layers.

1 18. The method of claim 11, wherein implanting dopants of a second
2 conductive type through the body contact windows comprises providing an amount of the
3 dopants to change a polarity of the first conductive type of the source regions into the second
4 conductive type.

1 19. The method of claim 11, wherein the isolation layer comprises silicate
2 glass.

1 20. The method of claim 11, wherein the first contact window is formed by
2 using the termination polysilicon layer as an etch stop layer.

1 21. The method of claim 11, wherein the source metal contact layer is
2 formed to have an edge beside the first contact window.

1 22. A semiconductor device set comprising at least one trench-typed
2 MOSFET and a trench-typed termination structure; wherein the trench-typed MOSFET has a
3 trench profile and comprises a gate oxide layer in the trench profile, and a polysilicon layer
4 on the gate oxide layer; wherein the trench-typed termination structure has a trench profile
5 and comprises an oxide layer in the trench profile, a termination polysilicon layer with
6 discrete features separating the termination polysilicon layer, an isolation layer covering the
7 termination polysilicon layer and filling the discrete features.

1 23. The semiconductor device set of claim 22, wherein the at least one
2 trench-typed MOSFET and the trench-typed termination structure are formed on a DMOS
3 device comprising an N+ silicon substrate, an N epitaxial layer on the N+ silicon substrate,
4 and a P epitaxial layer on the N epitaxial layer.

1 24. The semiconductor device set of claim 23, wherein the trench profiles
2 of the trench-typed MOSFET and of the trench-typed termination structure penetrate through
3 the P epitaxial layer into the N epitaxial layer.

1 25. The semiconductor device set of claim 23, wherein the DMOS device
2 further comprises a first P region located between the trench-typed termination structure and
3 the trench-typed MOSFET which is adjacent to the trench-typed termination structure, at
4 least one second P region located between the trench-typed MOSFETs, at least one N source
5 region surrounding the trench profiles.